CHAPTER FIVE

RTL NOR Gate

Digital Electronics.

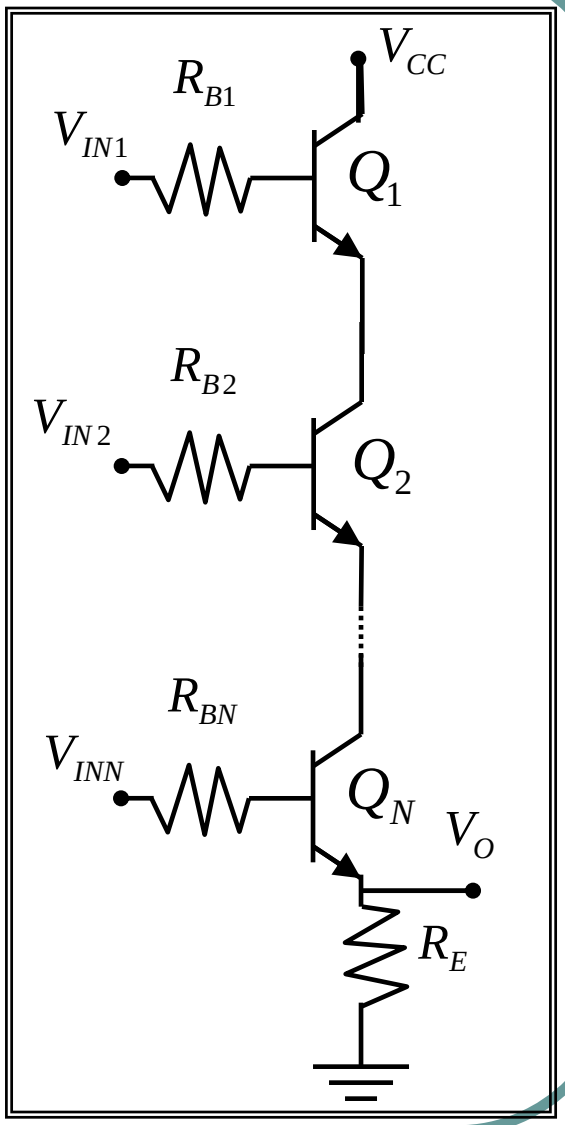
Basic RTL AND Gate

If at least one input less than V_{BE}(FA), then the corresponding Q is off. i.e. $I_E = 0$

$$V_{OL} = 0$$

If ALL inputs are greater than V_{IH}, then the corresponding Q is saturated.

$$V_{OH} = V_{CC} - N \times V_{CE}(sat)$$



RTL With Active Pull-Up Inverter

The object is to incresae the fan-out of RTL inverter gate (gives more current).

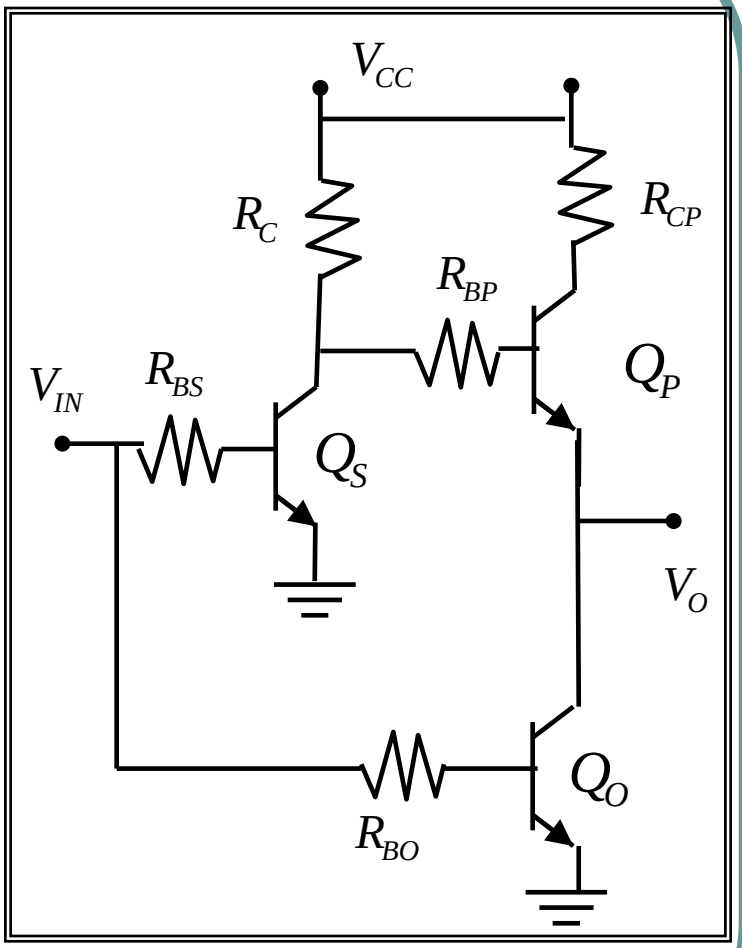
To accumplish active pull-up:

Basic assumptions: * $R_{CP} << R_C$

$R_{CP} \cong 0.1 \times R_C$

* $R_{BS} = R_{BO}$ and Q_O & Q_S turn ON and OFF simultaneously

* Q_S provides logic inversion for Q_P such that Q_S & Q_P never turn ON simutaneously



RTL With Active Pull-Up Inverter

For $V_{IN} \geq V_{INH}$ (Logic High)

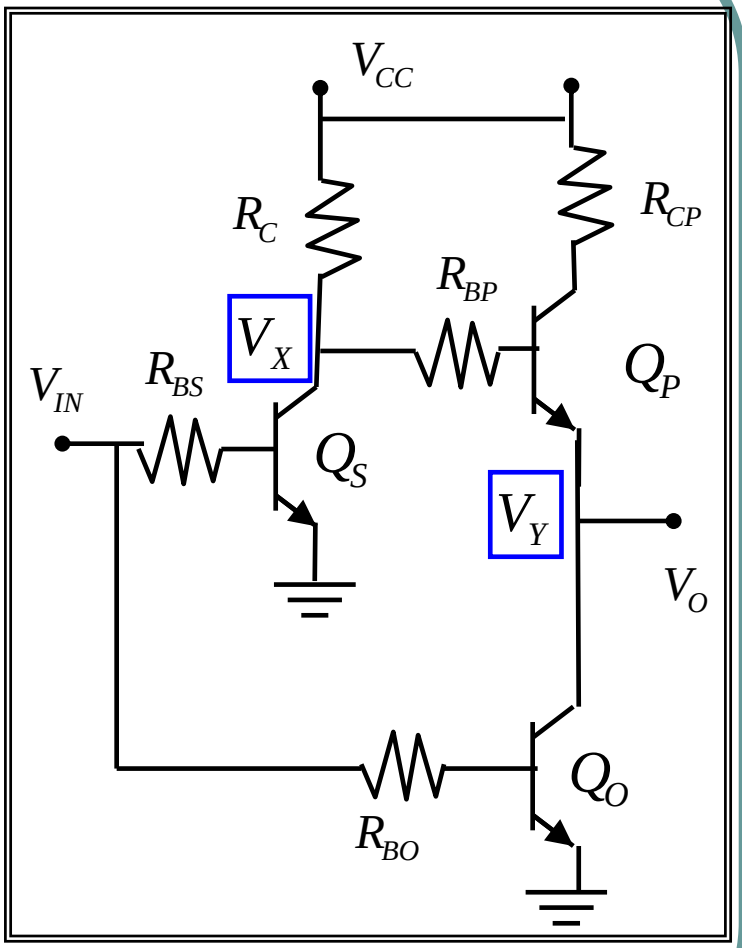
Q_O & Q_S are ON (sat) $V_X = V_Y = 0.2V$. → $V_X - V_Y < V_{BEP}$(FA). i.e. Q_P is cut-off (very very large resistance)

For $V_{IN} \leq V_{INL}$ (Logic Low)

Q_O & Q_S are cut-off

Q_P is ON (sat)

$$V_O = V_{CC} - V_{CE}(sat) - I_{CP}R_{CP}$$

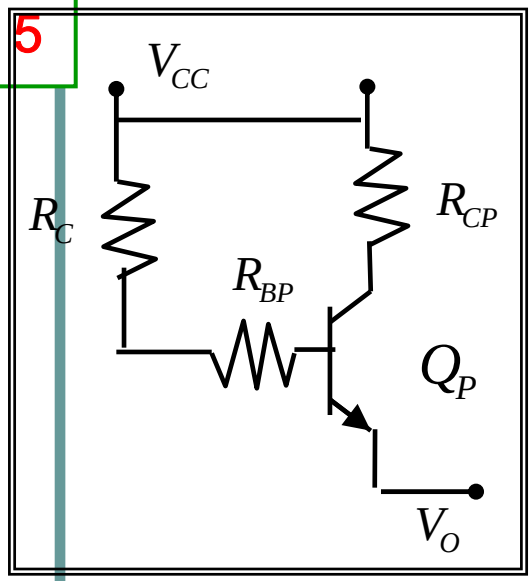


Fan-Out of RTL With Active Pull-Up Inverter

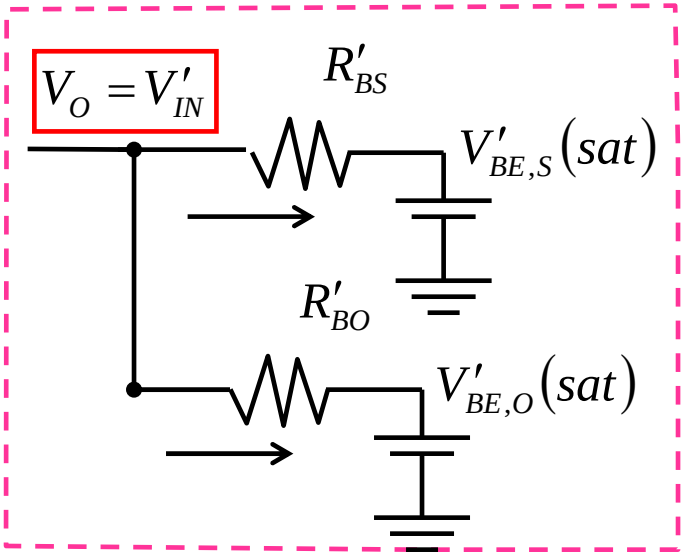
Fan-out is limited by the output high state of the driving gate

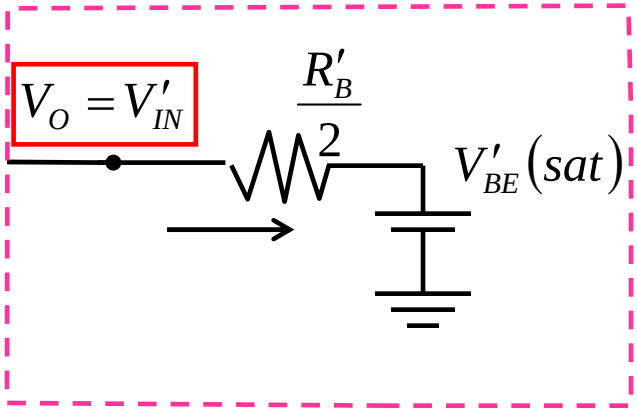
Q_O & Q_S are cut-off

Q_P is ON (sat)



Equivalent cct of driving gate when output is high





Equivalent cct of one load gate when input is high

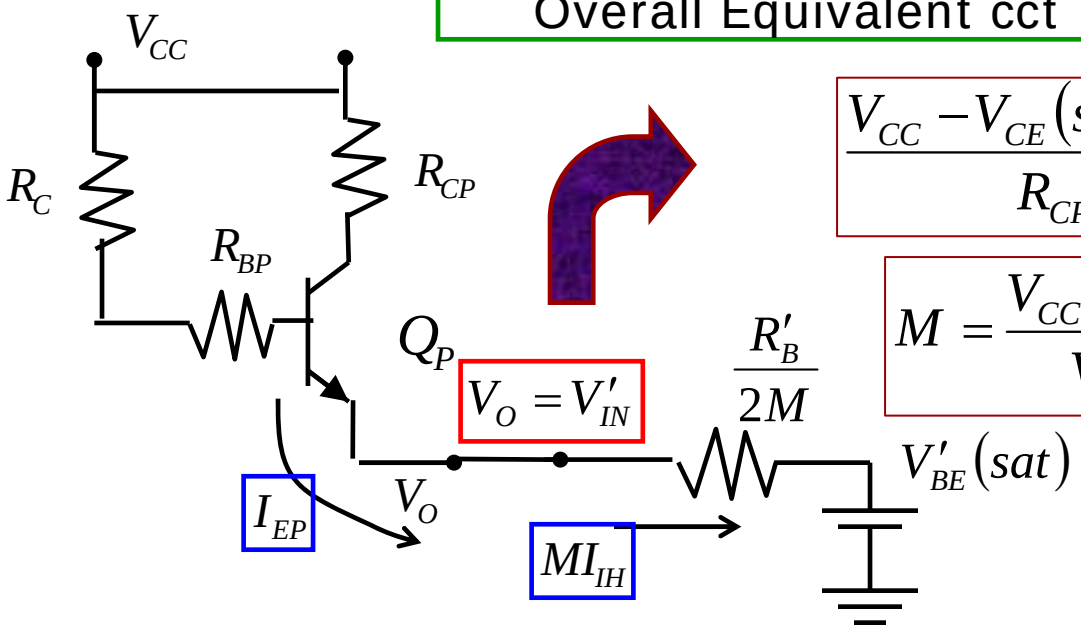
Fan-Out of RTL With Active Pull-Up Inverter

Fan-out is limited by the output high state of the driving gate

Q_O & Q_S are cut-off

Q_P is ON (sat)

Overall Equivalent cct



$$\frac{V_{CC} - V_{CE}(sat) - V_O}{R_{CP}} = \frac{V_O - V_{BE}(sat)}{R'_B / 2M}$$

$$M = \frac{V_{CC} - V_{CE}(sat) - V_O}{V_O - V_{BE}(sat)} \times \frac{R'_B}{2R_{CP}}$$

As M increases, I_{EP} increases, then V_O decreases

Fan-Out of RTL With Active Pull-Up Inverter

The limiting factor for V_O is that it must be sufficient to saturate Q_S' and Q_O' of the load gates.

It is easy to saturate Q_S since its effective load seen by the collector is very large with negligible I_C and I_B since Q_P is cut-off

i.e. to saturate Q_S , we need:

$$V_{OH}(\min) = V_{IH} = V_{BE}(sat) + \frac{R_B}{\beta_F}\left(\frac{V_{CC} - V_{CE,S}(sat)}{R_C}\right)$$

(Proved also in p. 10 of CH.4)

Substitute in

$$M = \frac{V_{CC} - V_{CE}(sat) - V_O}{V_O - V_{BE}(sat)} \times \frac{R'_B}{2R_{CP}}$$

Fan-Out of RTL With Active Pull-Up Inverter

- Example

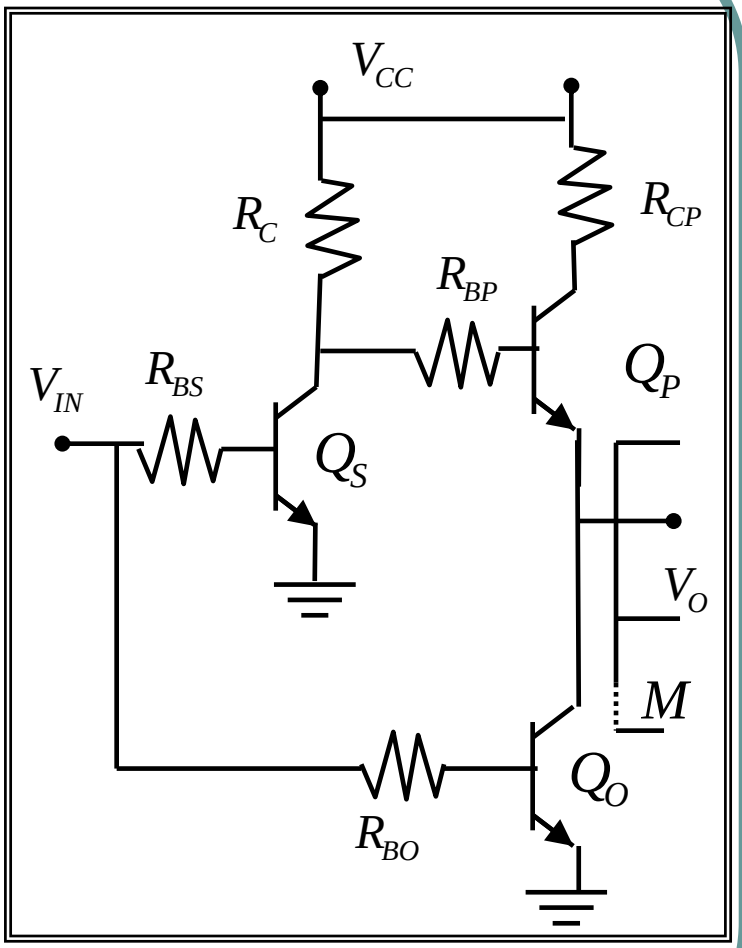
Determine the maximum fan-out for driving RTL gate, assuming $V_{CE}(sat)=0.2V$, $V_{BE}(sat)=0.8V$, $\beta_F=25, V_{CC}=5V, R_C=1k\Omega$, $R_{BO}=R_{BS}=10k\Omega, R_{CP}=100\Omega$.

- Solution

$$V_{OH}(\min)=0.8+\frac{10}{25}\left(\frac{5-0.2}{1}\right)=2.7V$$

$$M=\frac{5-0.2-2.7}{2.7-0.8}\times\frac{10}{2\times0.1}=55.3$$

$$M=55$$

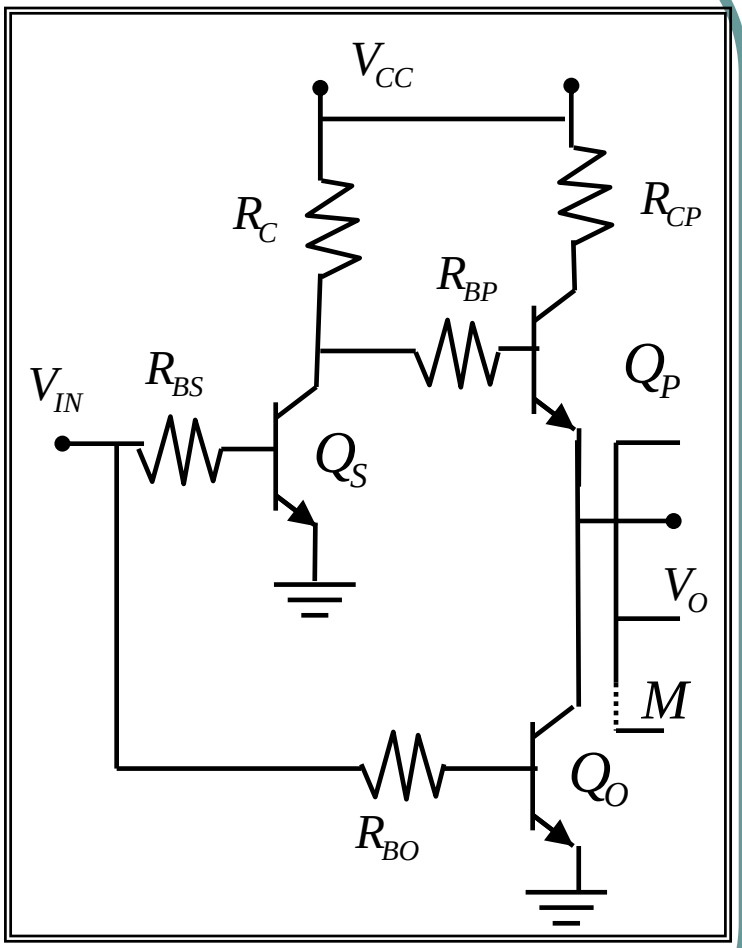


(without pull-up, M was 11. i.e. It increases 500%. See p. 10)

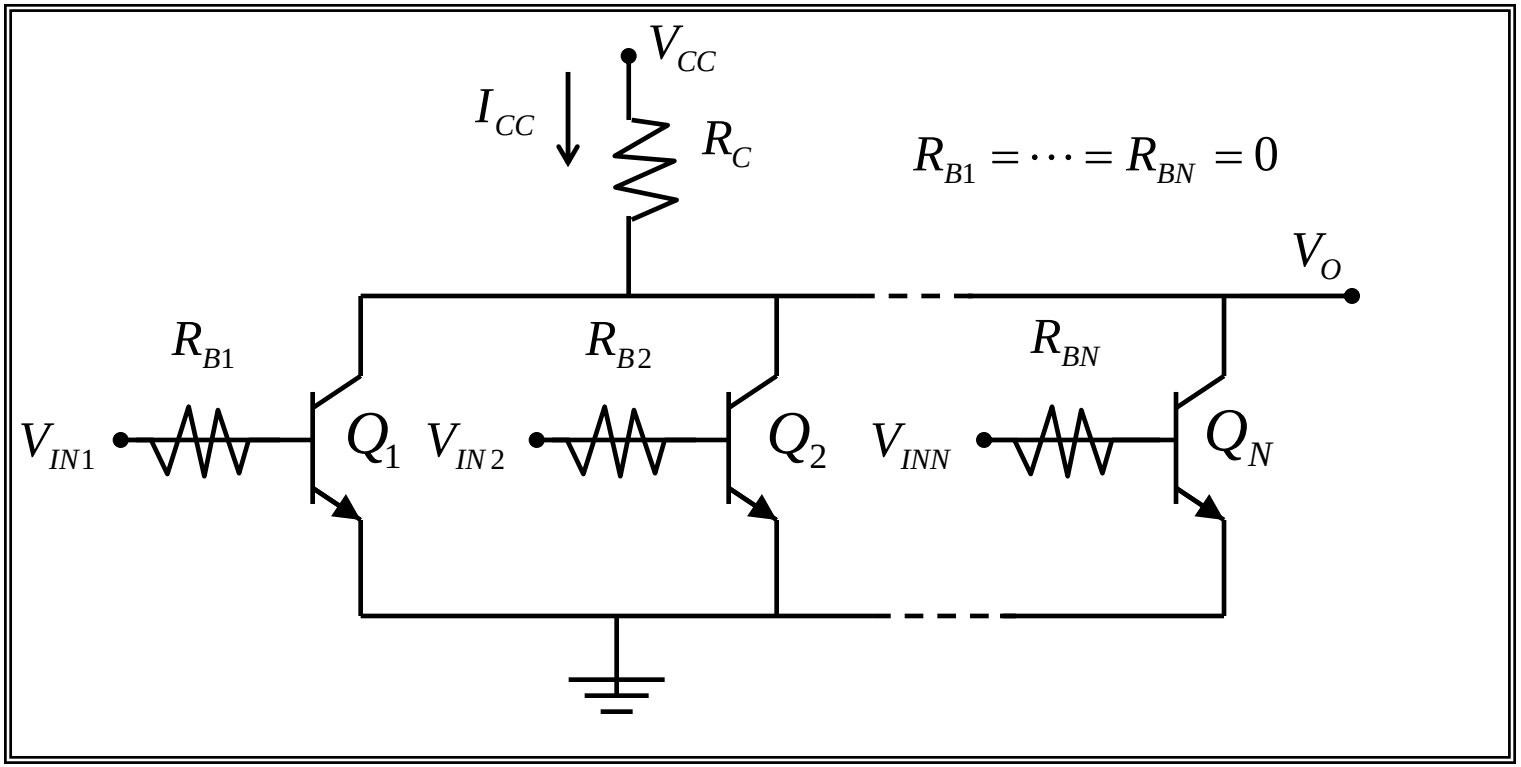
RTL SPICE Simulation

- Example

*Repeat the last example using PSPICE
*Plot V_O as a function of V_{IN}
*Refer to pages 67-68 in the text book.



Direct Coupled Transistor Logic



Three-input DCTL NOR gate

Advantage: Reduce the packing density of RTL in integrated circuits form since the base resistors are eliminated

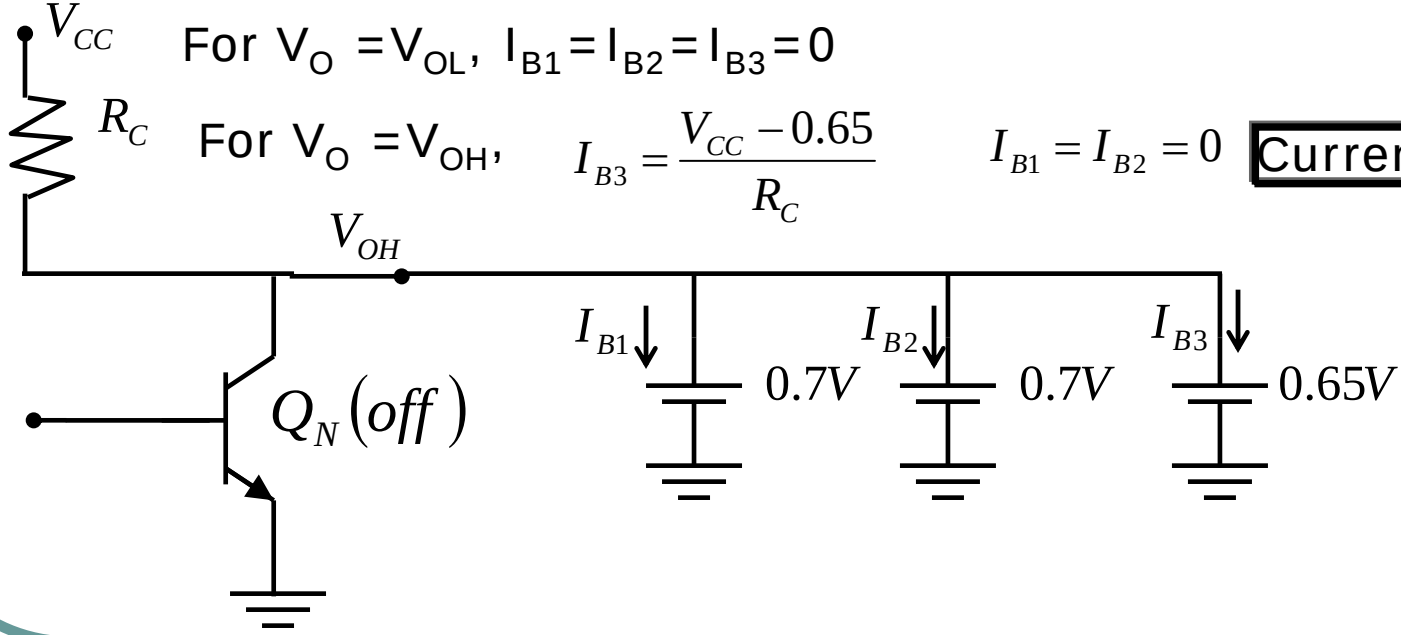
Disadvantage: Current hogging when V_O is at logic high for fan-out greater than one

Direct Coupled Transistor Logic

Example

Consider a DCTL RTL inverter with fan-out be three with $V_{BE1}(FA)=0.7V$, $V_{BE2}(FA)=0.7V$, $V_{BE3}(FA)=0.65V$.
Determine the base current of each load gate for output high state.

Solution



For $V_O = V_{OL}$, $I_{B1}=I_{B2}=I_{B3}=0$

For $V_O = V_{OH}$, $I_{B3}=\dfrac{V_{CC}-0.65}{R_C}$ $I_{B1}=I_{B2}=0$ Current hogging

- HW #5:Solve Problems: 5.8, 5.11, 5.22, 5.24, 5.27, 5.28, 5.29 (hint: neglect I_{BP})

- *Solutions of Prob. 5.24 & 5.27:*

  On the white board